Solutions - Homework 1

(Due date: January 24th @ 5:30 pm)
Presentation and clarity are very important!

PROBLEM 1 (25 PTS)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (9 pts)

✓ $F = A(C + \bar{B}) + \bar{A}$ ✓ $F = (Y + Z)(\bar{Y} + X)$ ✓ $F(X, Y, Z) = \prod(M_0, M_1, M_4, M_5)$

✓ $F = A(C + \bar{B}) + \bar{A} = (\bar{A} + C + \bar{B})(\bar{A} + A) = \bar{A} + C + \bar{B}$

✓ $F = (Y + Z)(\bar{Y} + X) = YX + \bar{Y}Z$

✓ $F(X, Y, Z) = \prod(M_0, M_1, M_4, M_5) = \sum(m_2, m_3, m_6, m_7) = \bar{X}Y\bar{Z} + \bar{X}YZ + XY\bar{Z} + XYZ$
$F(X, Y, Z) = \bar{X}Y(\bar{Z} + Z) + XY(\bar{Z} + Z) = \bar{X}Y + XY = Y.$

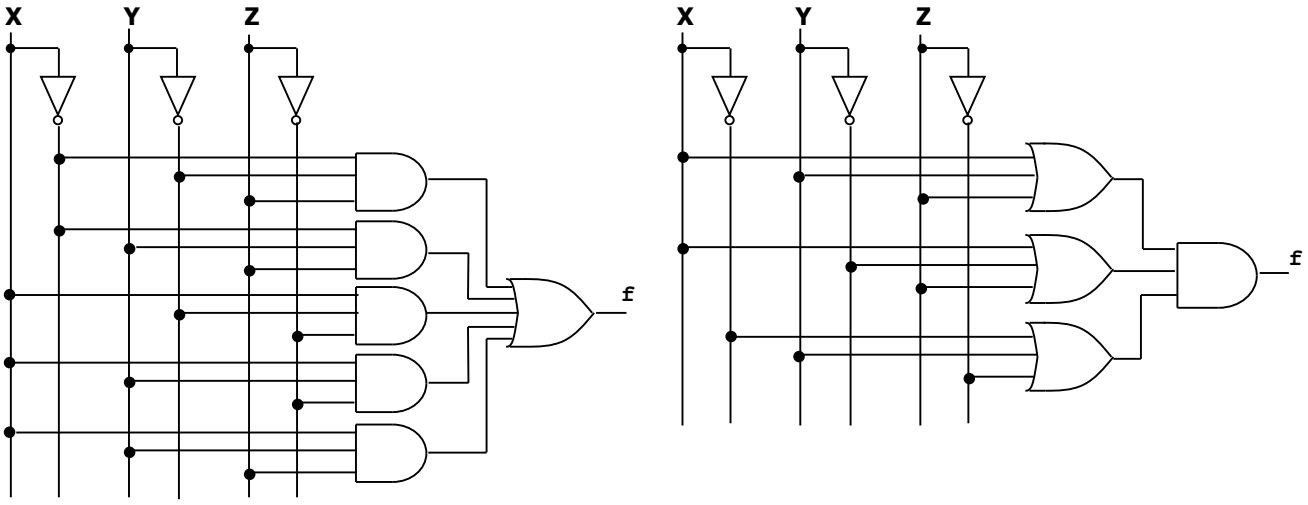
b) For the following Truth table: (6 pts)
- Provide the Boolean function using the Canonical Sum of Products (SOP), and Product of Sums (POS).
- Express the Boolean function using the minterms and maxterms representations.
- Sketch the logic circuit as Canonical Sum of Products and Product of Sums.

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

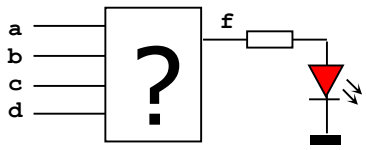
Sum of Products:
$f = \bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}\bar{Z} + XY\bar{Z} + XYZ$

Product of Sums:
$f = (X + Y + Z)(X + \bar{Y} + Z)(\bar{X} + Y + \bar{Z})$

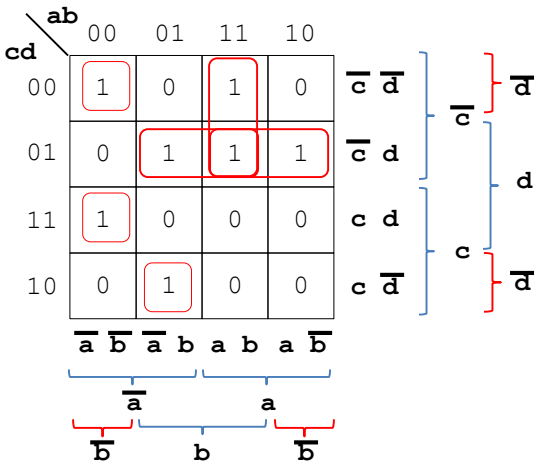
Minterms and Maxterms: $f = \sum(m_1, m_3, m_4, m_6, m_7) = \prod(M_0, M_2, M_5)$



c) Complete the truth table for a circuit (active high inputs, active high outputs) that activates an output (f='1') when the decimal value of the 4 inputs is equal to 0, 3, 5, 6, 9, 12, or 13. Then, simplify the function using Karnaugh maps. (10 pts)



a	b	c	d	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

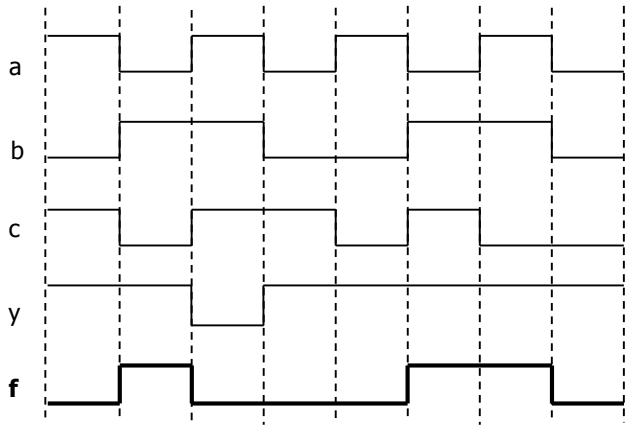


$f = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}cd + \bar{a}bc\bar{d} + ab\bar{c} + a\bar{c}d + b\bar{c}d = \bar{a}\bar{b}\overline{(c \oplus d)} + \bar{a}bc\bar{d} + ab\bar{c} + \bar{c}d(a + b)$

PROBLEM 2 (15 PTS)

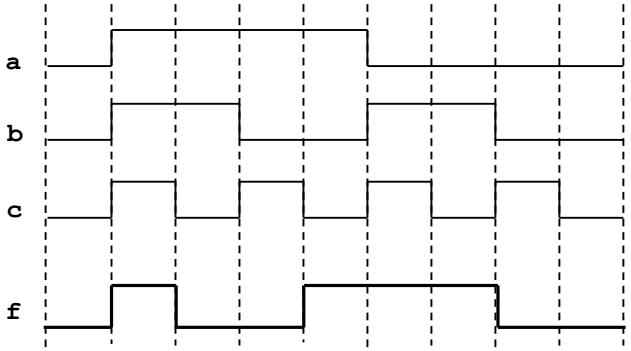
a) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture st of circ is
  signal x, y: std_logic;
begin
  x <= a and b;
  y <= x nand c;
  f <= y xor (not b);
end st;
```

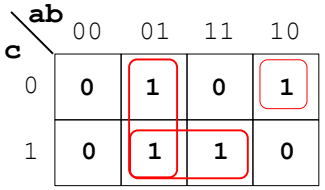


b) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (10 pts)

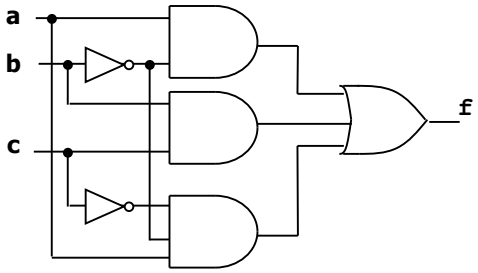
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
 port ( a, b, c: in std_logic;
        f: out std_logic);
end circ;

architecture st of circ is
  signal x, y, z: std_logic;
begin
  x <= not(a) and b;
  y <= c and b;
  z <= a and not(b) and not(c);
  f <= x or y or z;
end st;
```



a	b	c	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

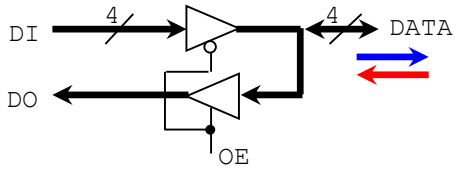


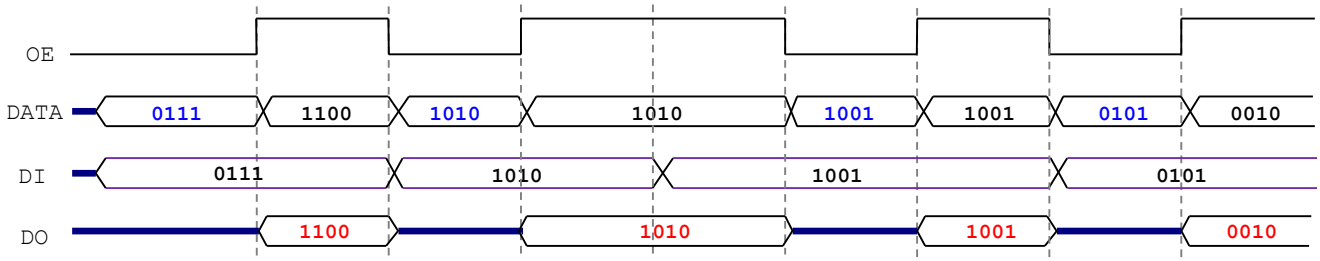
$f = \bar{a}b + cb + a\bar{b}\bar{c}$



PROBLEM 3 (10 PTS)

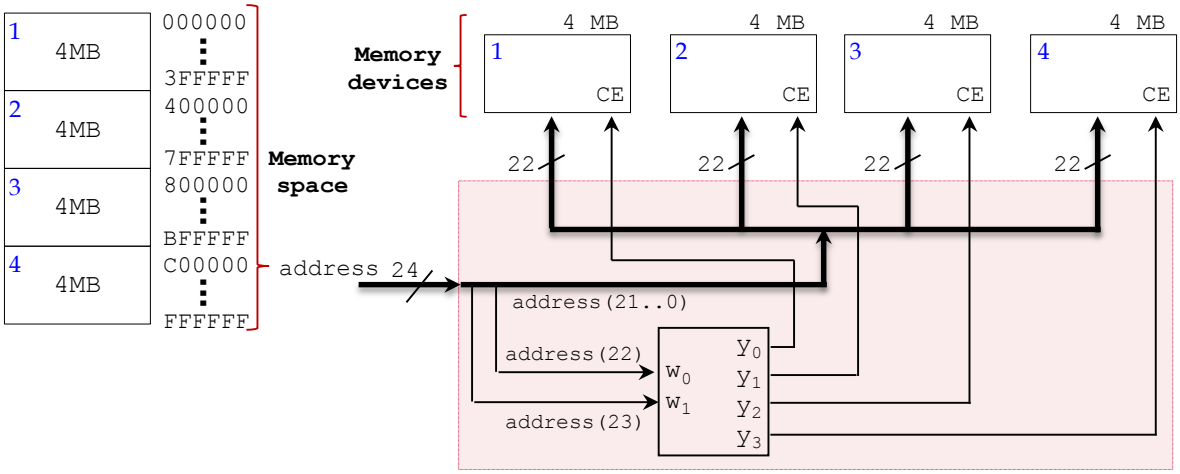
- For the following 4-bit bidirectional port, complete the timing diagram (signals DO and $DATA$):





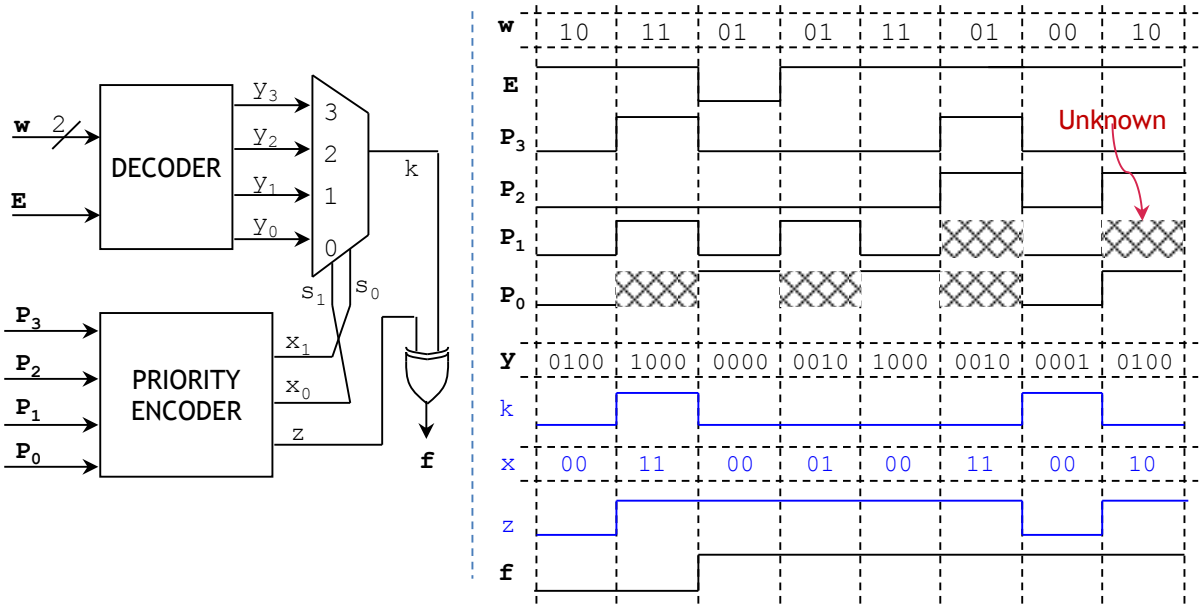
PROBLEM 4 (10 PTS)

- A 24-bit address line in a μprocessor handles up to $2^{24} = 16\,MB$ of addresses, each address containing one-byte of information. We want to connect four 4MB memory chips to the μprocessor.
- Sketch the circuit that: i) addresses the memory chips, and ii) enables only one memory chip (via CE: chip enable) when the address falls in the corresponding range. Example: if $address = 0x5FFFFF$, → only memory chip 2 is enabled (CE=1). If $address = 0xD00FA0$, → only memory chip 4 is enabled.
- Complete the number of bits '??' required for each 4MB memory chip.



PROBLEM 5 (15 PTS)

- Complete the timing diagram of the circuit shown below:



PROBLEM 6 (15 PTS)

- In these problems, you MUST show your conversion procedure.

a) Convert the following unsigned integer numbers to their binary and hexadecimal representation. (4 pts)
   - $124 = (1111100)_2 = 0x7C$
   - $115 = (1110011)_2 = 0x73$
   - $128 = (10000000)_2 = 0x80$
   - $255 = (11111111)_2 = 0xFF$

b) What is the minimum number of bits required to represent: (3 pts)
   - ✓ 50,000 colors? → $[log_2 50000] = 16\ bits$
   - ✓ 32679 symbols? $[log_2 32679] = 15\ bits$
   - ✓ 65536 memory addresses in a computer? → $[log_2 65536] = 16\ bits$

c) A microprocessor can handle addresses from `0x0000` to `0x1FFF`. How many bits do we need to represent those addresses? (2 pts).

```
0 0000 0000 0000: 0x0000
0 0000 0000 0001: 0x0001
      ...
      ...
      ...
1 1111 1111 1111: 0x1FFF
```

The range from `0x0000` to `0x1FFF` is akin to all the possible cases with 13 bits. So, we need **13 bits**.

d) Complete the following table. (6 pts)

Decimal	BCD	Binary number	Reflective Gray Code
128	0001 0010 1000	10000000	11000000
171	0001 0111 0001	10101011	11111110
49	0100 1001	110001	101001
241	0010 0100 0001	11110001	10001001
114	0001 0001 0100	1110010	1001011
631	0110 0011 0001	1001110111	1101001100

PROBLEM 7 (10 PTS)

- Complete the timing diagram of the digital circuit shown in the figure below. You must consider the propagation delays. Assume that the propagation delay of every gate is 5 ns. The initial values of the signals are specified in the figure.